IN THE SPECIFICATION:

Please amend paragraph **[001]** as follows:

[001] This application is a continuation of U.S. Patent Application Serial No. 09/012,388, filed on January 23, 1998, now abandoned. ~~which is incorporated herein by reference.~~

Please amend paragraph **[002]** as follows:

[002] The present invention relates to methods of forming an interconnect structure during integrated circuit fabrication. More particularly, the present invention relates to methods of forming a self-aligned interconnect structure for an integrated circuit. The method of the present invention is particularly useful in forming a ~~self-aligned~~ self-aligned polysilicon interconnect structure that can be sacrificially etched without damaging an adjacent active region that is provided with electrical communication through the interconnect structure.

Please amend paragraph **[003]** as follows:

[003] In the microelectronics industry, a substrate refers to one or more semiconductor layers or structures ~~which~~ that includes active or operable portions of semiconductor devices. In the context of this document, the term "semiconductor substrate" is defined to mean any construction comprising semiconductive ~~material, including~~ material including, but not limited ~~to~~ to, bulk semiconductive material such as a semiconductive wafer, either alone or in assemblies comprising other materials thereon, and semiconductive material layers, either alone or in assemblies comprising other materials. The term ~~substrate~~ "substrate" refers to any supporting structure ~~including~~ including, but not limited ~~to~~ to, the semiconductive substrates described above.

Please amend paragraph **[004]** as follows:

[004] Modern integrated circuits are manufactured by an elaborate process in which a large number of electronic semiconductor devices are integrally formed on a small

semiconductor substrate. The conventional semiconductor devices ~~which~~ that are formed on the semiconductor substrate include capacitors, resistors, transistors, diodes, and the like. In advanced manufacturing of integrated circuits, hundreds of thousands of these semiconductor devices are formed on a single semiconductor substrate.

Please amend paragraph **[008]** as follows:

[008] The active region is also becoming increasingly shallow. Consequently, measures must be taken in forming the interconnect structure and overlying semiconductor device to prevent silicon from the active region from being consumed. This shallowness of the active region often necessitates a planar interconnect structure interface that minimizes penetration of the original active region surface. The shallowness of the active region also often necessitates the use of a material other than the traditionally used aluminum in the interconnect structure for interfacing with the active region. Direct contact with aluminum causes the aluminum to diffuse into the silicon of the active region and to form spikes ~~which~~ that can penetrate entirely through the active region, causing adverse electrical consequences.

Please amend paragraph **[010]** as follows:

[010] One type of interconnect structure frequently used in the conventional technology is the buried contact. The buried contact is a region of polysilicon that makes direct contact between the interconnect structure and the active region, eliminating the need for a metal link. In forming the buried contact, a window is opened in a thin gate oxide over the active region that the interconnect structure is to electrically connect. Thereafter, polysilicon is deposited in direct contact with the active region in the opening but is isolated from the underlying silicon substrate of the semiconductor substrate by gate oxide and by field oxides everywhere else. An ohmic contact is formed at the polysilicon and active region interface by diffusion into the active region of a dopant present in the polysilicon. This dopant diffusion ~~in to~~ into the active region in effect merges the polysilicon with the active region. A layer of insulating film is then deposited to cover the buried contact.

Please amend paragraph **[012]** as follows:

[012] The buried contact also exhibits certain shortcomings. For instance, it is difficult at greater miniaturization levels to exactly align the contact hole with the active region when patterning and etching the contact hole. As a result, topographies near the active ~~are~~ region can be penetrated and damaged during etching of the contact hole. For example, a misaligned buried contact hole etch can notch ~~and therefore~~ and, therefore, damage a gate stack. The damage reduces the performance of the active region and neighboring ~~structures~~ structures, which causes a loss of function of the semiconductor device being formed and possibly a defect condition in the entire integrated circuit. To remedy the problems associated with the buried contact, the prior art uses compensation techniques such as an etch stop barrier. These compensation techniques are time consuming and thus reduce throughput.

Please amend paragraph **[015]** as follows:

[015] Further advantages of this method include a low contact resistance and a large area of contact between the active region and the silicide. Nevertheless, the ~~self-aligned~~ self-aligned silicide contact also has drawbacks in that it requires numerous steps to form, reducing integrated circuit fabrication throughput. It also consumes a significant portion of the active region in being formed and cannot be sacrificially etched without harming the active region.

Please amend paragraph **[017]** as follows:

[017] The conventional self-aligned silicide contact cannot be used as a landing pad. A further shortcoming of using the landing pad is that it is not always possible to conduct the sacrificial etching evenly across the whole semiconductor substrate. The center of the semiconductor substrate, in many instances, is etched at a faster rate than the edges. Thus, landing pads located at the center of the semiconductor substrate may be etched through, allowing the etching process to come in contact with the active region before landing pads at the edges of the semiconductor substrate are sufficiently etched. As a consequence, damage to active regions at the center of the semiconductor substrate can occur. Accordingly, an interconnect

structure that can function as a sacrificial landing pad, that can be self aligned, and that effectively protects the active region against ~~overetching~~ over-etching is also needed in the art.

Please amend paragraph **[021]** as follows:

[021] In accordance with the invention as embodied and broadly described herein in the preferred embodiment, a sacrificial, self-aligned polysilicon interconnect ~~structure~~ structure, as well as a method for constructing the sacrificial, self-aligned polysilicon interconnect ~~structure~~ structure, are provided. The method involves the utilization of mechanical polishing and stop-on-feature trench isolation in order to form the sacrificial, ~~self-aligned~~ self-aligned polysilicon interconnect.

Please amend paragraph **[024]** as follows:

[024] Once the nitride layer is formed, a region of insulating ~~material~~ material, which, in one embodiment forms an isolation region, is created by etching a trench through the nitride layer and the sacrificial oxide layer and then filling the trench with a conformal dielectric film. In one embodiment, the conformal dielectric film comprises an oxide film.

Please amend paragraph **[034]** as follows:

[034] The vertically extending segment is preferably doped after the buried contact is formed. A semiconductor device is then typically constructed over the exposed active region contacting a top surface of the active region. In one ~~embodiment~~ embodiment, the semiconductor device is a DRAM container capacitor cell that is constructed over the buried contact. In constructing the container capacitor cell, a gate oxide region is first formed at the surface of the active region. Typically, several gate regions are then formed over the active region. The gate regions provide control signals to the container capacitor cell during integrated circuit operation and serve as guides for aligning the container capacitor cell during the formation thereof. Next, the container capacitor cell is patterned and formed over the buried contact. The buried contact serves as a sacrificial landing pad for the container capacitor cell formation process and, due to

its unique structure, protects the active region against over-etching. The buried contact serves as a base for the container capacitor cell and, because it is encased in the ~~non-conductive~~ non-conductive isolation region, also prevents charge leakage from the container capacitor cell.

Please amend paragraph **[037]** as follows:

[037] A more particular description of the invention briefly described above will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are ~~not therefore~~ not, therefore, to be considered limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

Please amend paragraph **[046]** as follows:

[046] Figure 1 illustrates an initial step of the method of the present invention. In the initial step, a substrate assembly is provided on which sacrificial self-aligned interconnects will be formed. As defined herein, a substrate assembly comprises a substrate on which may be formed one or more structural layers. In the depicted embodiment, the substrate assembly comprises a substrate assembly ~~10,~~ 10 and a silicon substrate 12 is provided on substrate assembly 10. Shown by way of example in silicon substrate 12 is a vertically extending segment 14 of silicon substrate 12 where a pair of active regions are intended to be later formed. In the course of fabrication of an integrated circuit, the active regions are required to be placed in electrical communication with an overlying semiconductor ~~device,~~ device and the sacrificial self-aligned interconnects will be used for doing so.

Please amend paragraph **[047]** as follows:

[047] In the depicted embodiment, the method of the present invention is used to form a particular type of interconnect structure known as the buried contact. Two buried contacts are shown being formed, each connecting one of two vertically extending segments 14 with a

separate overlying semiconductor device in the form of a container capacitor cell. While the formation of two buried contacts electrically connecting two vertically extending segments 14 with two overlying container capacitor cells is illustrated, nevertheless, only one interconnect structure need be formed at a time ~~and~~ and, of course, more than two could also be formed. Furthermore, varying types of interconnect structures other than a buried contact could also be formed with the method of the present ~~invention,~~ invention and the semiconductor substrate assembly 10 could be other than the depicted container capacitor cells.

Please amend paragraph **[049]** as follows:

[049] In a further step of the method of the present ~~invention~~ invention, a sacrificial covering layer is formed over vertically extending segments 14. In the depicted embodiment, the sacrificial covering layer comprises a nitride layer 18 which is composed of silicon nitride. In addition to nitride layer 18, other additional protective layers may also be deposited. For instance, in the depicted ~~embodiment~~ embodiment, a sacrificial oxide layer 16 is formed prior to the deposition of nitride layer 18. Sacrificial oxide layer 16 is used to protect underlying vertically extending segments 14 and silicon substrate 12 from damage during a subsequent step of removing nitride layer 18. Of course, if a process for removing nitride layer 18 is selected that does not require an additional protective layer, the formation of sacrificial oxide layer 16 can be eliminated. Any suitable process can be used for forming sacrificial oxide layer 16 and nitride layer 18.

Please amend paragraph **[054]** as follows:

[054] As a remedy to the problem of misalignment of a contact hole, and in accordance with the method of the present invention, a stop-on-feature etching process is used to etch contact holes 24a and 24b that selectively etches oxide at a faster rate than the etching process etches nitride layer 18. Of course, if a sacrificial covering layer other than nitride layer 18 is used, an etching process that is selective to the particular material of the sacrificial covering layer used would then be employed. As a result of the use of the stop-on-feature etching ~~process,~~ process and the arrangement provided by the present invention wherein

vertically extending segments 14 are covered and protected by nitride layer 18, the buried contact etching process self-aligns contact holes 24a and 24b each to an adjacent edge 28 of one of vertically extending segments 14 without causing damage to vertically extending segments 14.

Please amend paragraph **[055]** as follows:

[055] As a consequence of the ~~forgoing,~~ foregoing, the preexisting geometry of vertically extending segments 14 is maintained and, as a result of the predictability provided thereby, the integrated circuit can be designed with reduced dimensions of vertically extending segments 14. This in turn allows for greater miniaturization of the integrated circuit. Also, the greater accuracy of the stop-on-feature etching process results in a higher yield rate due to better electrical characteristics resulting from the predictability of the geometry.

Please amend paragraph **[056]** as follows:

[056] In the depicted embodiment, a stop-on-feature etching process is selected that selectively etches oxide at a faster rate than the etching process etches nitride. Such etching processes are well known in the art, but as an example, one such etching process comprises a ~~plasma-generated~~ plasma-generated reactive ion etching (RIE) process. The manner of conducting the RIE etching process to selectively etch oxide at a faster rate than it etches nitride is described in U.S. Patent Number 5,286,344, which is hereby incorporated by reference into this document.

Please amend paragraph **[060]** as follows:

[060] As shown in Figure 6, after filling contact holes 24a and 24b, the surface of substrate assembly 10 is polished back to the level of nitride layer 18. Polishing back can be conducted by an etchback process or by any form of mechanical polishing, though in the depicted embodiment, polishing back is conducted with CMP. CMP is preferred for polishing back due to the X-Y anisotropy provided therewith. In the depicted embodiment, a CMP process is used which etches oxide and polysilicon, but which stops on nitride. One example ~~is of~~ of such a

CMP process is the use of a polyurethane pad and a KOH or ~~ammonia based~~ ammonia-based silicate slurry.

Please amend paragraph **[062]** as follows:

[062] The result of the ~~forgoing~~ foregoing polishing back step is that contact holes 24a and 24b now form buried contacts 32a and 32b, both of which are aligned to corresponding adjacent edge 28 of vertically extending segments 14. Accordingly, even though misaligned contact hole 24b seen in Figure 4 was etched with a slight misalignment, it has been aligned by the method of the present invention to corresponding adjacent edge 28 of one of vertically extending segments 14 as shown in buried contact 32b of Figure 6. The self-alignment of buried contact 32b is enabled by the use of the stop-on-feature etching process together with nitride ~~layer 18~~ layer 18, which blocks the stop-on-feature etching process from etching vertically extending segments 14. It is also enabled by the planarization process that removes a portion of misaligned contact hole 24b that was etched over nitride layer 18.

Please amend paragraph **[063]** as follows:

[063] In a further step of the method of the present invention, nitride layer 18 is removed. One manner of removing nitride layer 18 is with a hot phosphoric acid stripping process. In order to keep the polysilicon in buried contacts 32a and 32b clean from contamination by the hot phosphoric acid stripping process, buried contacts 32a and 32b are first capped with oxide. This is done by exposing buried contacts 32a and 32b to oxygen at an elevated temperature to form thin grown oxide layers in the form of oxide caps 34 over each of buried contacts 32a and 32b. The hot phosphoric acid nitride stripping process is then conducted without contaminating the polysilicon in buried contacts 32a and 32b to result in the structure of Figure 7. The hot phosphoric acid stripping process is convenient in that it can be easily incorporated into existing process flows. Consequently, the method of the present invention can be easily integrated into existing fabrication ~~processes~~ processes, effectively and with a minimum of expense.

Please amend paragraph **[064]** as follows:

[064] After nitride layer 18 is removed, sacrificial oxide layer 16 and oxide caps 34 are also removed ~~with~~ using a suitable process. Vertically extending segments 14 and buried contacts 32a and 32b are at this stage exposed and prepared for the construction of an overlying semiconductor device over the top of each thereof.

Please amend paragraph **[065]** as follows:

[065] While vertically extending segments 14 could be contacts, gate regions, or other conductive structures with a vertical sidewall, in the depicted ~~embodiment~~ embodiment, vertically extending segments 14 will be doped to form active regions. Doped active regions 48 are shown in Figure 8. Vertically extending segments 14 are preferably doped after formation of isolation region 26 to form active regions 48. This will allow active regions 48 to be self-aligned to the edges of isolation region 26.

Please amend paragraph **[066]** as follows:

[066] Figure 8 illustrates the forming of the overlying semiconductor device, which, in the depicted ~~embodiment~~ embodiment, is a set of container capacitor cells. In forming the container capacitor cells, a fresh gate oxide layer 38 is first deposited, and gate regions 40 are then formed above buried contacts 32a and 32b. Gate regions 40 provide control signals to the container capacitor during integrated circuit operation and serve as guides for aligning the container capacitor cell during container capacitor cell formation. Gate regions 40 are subsequently encased in insulating spacers such as oxide spacers 42, after which container capacitor storage nodes 44 are deposited and patterned over buried contacts 32a and ~~32b~~ 32b, using gate regions 40 for alignment. Buried contacts 32a and 32b serve as landing pads for container capacitor storage nodes 44.

Please amend paragraph **[067]** as follows:

[067] In forming container capacitor storage nodes 44 or other overlying semiconductor devices, it is often necessary to use buried contacts 32a and 32b as sacrificial

landing pads. When doing so, buried contacts 32a and 32b may need to be sacrificially etched. The present invention provides a means for preserving the geometry of active regions 48 from damage when sacrificially etching buried contacts 32a and 32b. One example of a means for preserving active regions 48 from damage is the placement of buried contacts 32a and ~~32b~~ 32b, each to the side of one of active regions 48. Nitride layer 18 can also be left in place to protect active regions 48 from damage when etching buried contacts 32a and 32b as a further means for preserving active regions 48 from damage when sacrificially etching buried contacts 32a and 32b.

Please amend paragraph **[069]** as follows:

[069] Underlying portion 36 of isolation region 26 allows extreme over-etch and, as a result, buried contacts 32a and 32b can be etched to as great a degree as necessary. An over-etch that etches into underlying portion 36 of isolation region 26 is prevented by underlying portion 36 from damaging either of silicon substrate 12 or active regions 48. This adds toleration to the process flow and is particularly useful when it becomes necessary to etch deeply into a landing pad. It is also particularly useful when using an etching process that etches portions of substrate assembly 10 at a faster rate ~~(e.g.~~ (e.g., at the center thereof) than other portions ~~(e.g.~~ (e.g., at the edge thereof).

Please amend paragraph **[071]** as follows:

[071] The present invention provides a unique interconnect structure which is ~~self-aligned~~ self-aligned and which can be sacrificially etched due to the step of taking a horizontal interconnect structure from the prior art and causing it to have a planar vertical interface. Shown in Figure 7 are two such interconnect structures that comprise buried contacts 32a and 32b. Each of buried contacts 32a and 32b comprises a vertically extending plug of electrically conductive material formed in isolation region 26 at an edge 28 of one of active regions 48. Each of buried contacts 32a and 32b contacts at one side thereof a vertical segment of one of active regions 48 with a planar vertical interface. A top surface of each of buried contacts 32a and 32b electrically contacts one of overlying container capacitor storage nodes 44. Container capacitor storage

nodes 44 are in electrical communication with one of active regions 48 only through one of buried contacts 32a and 32b.